WHAT IS CLAIMED IS:

1. A method of fabricating an X-ray detector array, comprising the steps of:

providing a substrate having a capacitor area and a transistor area;

forming a gate line transversely extending on the substrate, wherein the gate line includes a gate electrode in the transistor area;

forming a gate insulation layer on the gate line, the gate electrode and the substrate;

forming a semiconducting island on the gate insulation layer in the transistor area;

forming a common line and a data line longitudinally extending on the gate insulation layer, and forming a source electrode and a drain electrode on the semiconducting island to form a thin film transistor (TFT) structure, wherein the drain electrode electrically connects the data line;

forming a first conductive layer on the gate insulation layer in the capacitor area and to cover the common line;

forming a conformal passivation layer on the gate insulation layer, the first conductive layer, the TFT structure, the data line and the gate line;

forming a first via hole penetrating the passivation layer to expose the surface of the source electrode;

forming a planarization layer on the passivation layer and filling the first via hole;

forming a second via hole and a third via hole penetrating the planarization layer, wherein the second via hole exposes at least the surface of the source electrode, and the third via hole exposes the surface of the passivation layer in the capacitor area; and

forming a conformal second conductive layer on part of the planarization layer and electrically connecting the source electrode;

wherein a storage capacitor structure is composed of the first conductive layer, the passivation layer and the second conductive layer in the capacitor area.

2. The method according to Claim 1, wherein the gate line is metal.

3. The method according to Claim 1, wherein the gate insulation layer is $SiO_2$, $SiN_x$ or SiON.

4. The method according to Claim 1, wherein the method of forming the semiconducting island comprises the steps of:

forming an amorphous silicon layer on the gate insulation layer;

forming a doped amorphous silicon layer on the amorphous silicon layer; and

removing part of the doped amorphous silicon layer and the amorphous silicon layer to form the semiconducting island in the transistor area.

5. The method according to Claim 4, further comprising, after the step of forming the common line, the data line and the TFT structure, the step of:

using the source electrode and drain electrode as a mask, and removing part of the doped amorphous silicon layer to expose the surface of the amorphous silicon layer.

6. The method according to Claim 1, wherein the common line, the data line, the source electrode and the drain electrode are simultaneously defined by photolithography.

7. The method according to Claim 1, wherein the first conductive layer is indium tin oxide (ITO) or indium zinc oxide (IZO), serving as a bottom electrode or a pixel electrode.

8. The method according to Claim 1, wherein the passivation layer is dielectric.

9. The method according to Claim 8, wherein the passivation layer is $SiN_x$.

10. The method according to Claim 1, wherein the planarization layer is a spin-on-glass (SOG) layer or organic layer.

11. The method according to Claim 1, wherein the second conductive layer is indium tin oxide (ITO) or indium zinc oxide (IZO), serving as a top or charge collector electrode.

12. The method according to Claim 1, wherein the gate line has a protruding portion in the transistor area serving as the gate electrode.

13. The method according to Claim 1, wherein the gate line located in the transistor area serves as the gate electrode.

14. A method of fabricating an X-ray detector array, comprising the steps of:

providing a substrate having a capacitor area and a 4 transistor area;

forming a gate line transversely extending on the substrate, wherein the gate line includes a gate electrode in the transistor area;

forming a gate insulation layer on the gate line, the gate electrode and the substrate;

forming asemiconducting layer on the gate insulation layer;

forming a first conductive layer on the semiconducting layer;

using a gray-tone photolithography, removing part of the first conductive layer and the semiconducting layer to form a common line longitudinally extending on a first semiconducting island, and a source electrode, a drain electrode and a longitudinally extending data line on a second semiconducting island thereby forming a thin film transistor (TFT) structure, wherein the drain electrode electrically connects the data line;

forming a second conductive on the gate insulation layer in the capacitor area and to cover the common line;

forming a conformal passivation layer on the gate insulation layer, the second conductive layer, the TFT structure, the data line and the gate line;

forming a first via hole penetrating the passivation layer to expose the surface of the source electrode;

forming a planarization layer on the passivation layer and filling the first via hole;

forming a second via hole and a third via hole penetrating the planarization layer, wherein the second via hole exposes at least the surface of the source electrode, and the third via hole exposes the surface of the passivation layer in the capacitor area; and

forming a conformal third conductive layer on part of the planarization layer and electrically connecting the source electrode;

wherein a storage capacitor structure is composed of the second conductive layer, the passivation layer and the third conductive layer in the capacitor area.

15. The method according to Claim 14, wherein the gate line is metal.

16. The method according to Claim 14, wherein the gate insulation layer is $SiO_2$, $SiN_x$, or SiON.

17. The method according to Claim 14, wherein the first conductive layer is metal.

18. The method according to Claim 14, wherein the method of forming the semiconducting layer comprises the steps of:

forming an amorphous silicon layer on the gate insulation layer; and

forming a doped amorphous silicon layer on the amorphous silicon layer.

19. The method according to Claim 18, further comprising, after the step of forming the common line, the data line and the TFT structure, the step of:

using the source electrode and drain electrode as a mask, and removing part of the doped amorphous silicon layer to expose the surface of the amorphous silicon layer.

20. The method according to Claim 14, wherein the second conductive layer is indium tin oxide (ITO) or indium zinc oxide (IZO), serving as a bottom electrode or a pixel electrode.

21. The method according to Claim 14, wherein the passivation layer is dielectric.

22. The method according to Claim 21, wherein the passivation layer is $SiN_x$.

23. The method according to Claim 14, wherein the planarization layer is a spin-on-glass (SOG) layer or organic layer.

24. The method according to Claim 14, wherein the third conductive layer is indium tin oxide (ITO) or indium zinc oxide (IZO), serving as a top or charge collector electrode.

25. The method according to Claim 14, wherein the gate line has a protruding portion in the transistor area serving as the gate electrode.

26. The method according to Claim 14, wherein the gate line located in the transistor area serves as the gate electrode.